A 0.18 µm Flash Source Side Erasing Improvment

R. Laffont[1], R. Bouchakour[1],O. Pizzuto[2], J.M Mirabel[2]
1 L2MP-Polytech, UMR CNRS 6137, IMT Technopole Château Gombert, 13451 Marseille – France
phone : +33 491 054 777 / fax : +33 491 054 782 / email : romain.laffont@polytech.univ-mrs.fr
[2] ST-Microelectronics, ZI Rousset BP 2, F-13106 Rousset CEDEX, France

Introduction

The requirement of high density memories with low power consumption, particularly for portable systems, makes flash EEPROM's possible candidates for RAM operation avoiding the need of frequent data refresh [1]. For this purpose, the long erasing time required when Fowler–Nordheim (FN) tunneling is used to modify the charge stored in the floating gate (FG) is considered to be one of the main disadvantages. In this paper, we present two solutions to improve 0.18 µm Flash erasing obtained with our Flash compact model [2].

Cell modeling

This model is a compact floating gate memory model which can be used to analyse cell electrical behaviour, to improve cell design and also to create some new memories structures. It has been developed in hardware description language analog (HDLA) to be used in common circuit simulators (Eldo). With this model, we can simulate both transient and static characteristics. MOSFET description based on Pao and Sah approach, allows the physical parameters continuity between all regimes and the channel spatial resolution of electrical field and inversion charge. This model has been applied to Flash memory cell to investigate the dynamic behaviour of important variables such as tunnelling current amplitudes during the writing and erasing operations. To validate our model, transient threshold voltage variations during the writing and erasing operations have been measured and compared to simulations [2]. Figure 1 presents a dynamic erasing current simulation from the floating gate to the source (I_{FNs}) and channel (I_{FNb}) regions. This simulation shows a small source current contribution for the total erasing current because the floating gate overlap area is smaller than the channel one. We can see also that effective injection current occurs only during 200 ms of cell time erasing (350 ms). From this remarks we propose two solutions to improve Flash cell erasing.

Signal optimisation

First solution based on simulation obtained with our Flash model proposed new erasing signal. Signal is calculted for erasing constant current injection [3]. Figure 2 compare standard (350ms) and 80 ms optimized signal obtained in simulation for the same final threshold volatge. Optimized signal has been validated with 0.18µm Flash technologie processed by ST-Microelectronics. Figure 3 compare simulation and measure transient threshold voltage with optimized signal. We can see good corelation between our simulation and measure. Table I compare erase threshold voltage obtained on same cell with standard and optimized signal.

TABLE I

Erase threshold voltage with standard and optimzed signal

Signal	V_{TERASE} (V)
Standard 350ms, V_{MAX} = 7V	2.73
Optimized 80 ms , V_{MAX} = 7.8V	2.7

This result show that is possible to reduce by a factor 4 time erasing with only an voltage increase in 0.8V.

Process optimization (Patent ST-Microelecronics) [4]

Figure 4 present a SEM picture of a standard Flash designed by ST-Microelectronics where source and drain area are shown. After cell process flow study, in particulary Self Aligned Source operation (SAS), we have proposed a very simple modification of this flow to increase floating gate overlap region on source cell. Figure 5 present cell after source self aligned etching. This figure show a polymer layer obtained during etching. In classical process flow, the implant cell source is directly done after SAS etching, so through polymer. Here we propose to withdraw resin (and polymer) before source implant. Table II compare classical and modified flow process for SAS operation.

TABLE II

Flow process

Standard	Modified flow
Resin deposit	Resin deposit
SAS etching	SAS etching
Source implant	Withdrawal resin
Withdrawal resin	Source implant

Figure 6 compare transient threshold voltage variation during erasing for cell processsed with classical and optimized process. This first electrical results expose an improvement of injection effeciency for the modified process.

Conclusion

In this work, we have demonstrated that it's possible to reduce the erasing time of 0.18 µm Flash. To reach this goal, we have developed a physical compact model of a Flash memory cell to investigate the dynamic behavior of main cell electrical parameters such as tunnelling current. A new signal and modified process has been proposed and validated with ST-Microelectronics Flash technologie.

References

[1] W.D. Brown, J.E. Brewer, IEEE, New York, 1998.
[2] Laffont, P. Masson, S. Bernardini, R. Bouchakour, J.M. Mirabel, *Journal of Non-Crystalline Solids*, 2003, Vol. 322, Issues 1-3, p. 250-255
[3] P. Canet, R. Bouchakour, N. Harabech, Ph. Boivin, J.M. Mirabel, C. Plossu, 43rd IEEE Symposium on Circuits and Systems, Lansing, Michigan, August 8–11, 2000.
[4] O. Pizzuto, R. Laffont, J.M. Mirabel, patent ST-Microelectronics n°02-RO-250, Patent US extension in progress

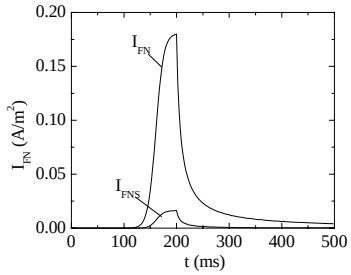

Figure 1: Dynamic erasing currents simulation from the floating gate to the source (I_{FNs}) and channel (I_{FNb}) regions

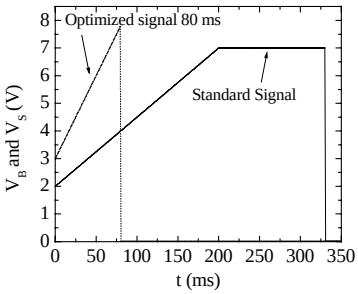

Figure 2: Optimized and classical erase signal applied on source and substrate

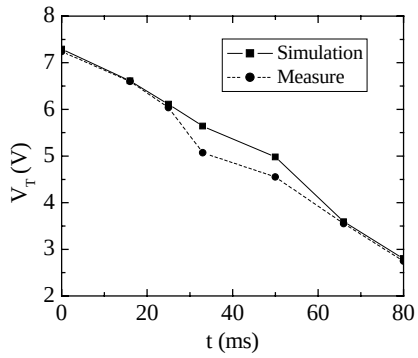

Figure 3: Comparison between simulation and measurement of the threshold voltage with optimized signal.

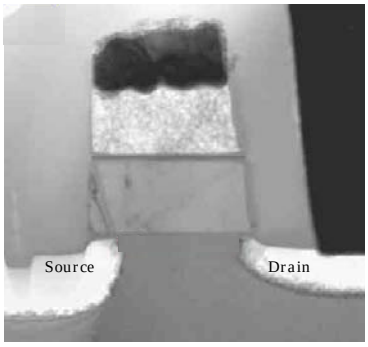

Figure 4: Source and drain area obtained with SEM picture of a Flash cell

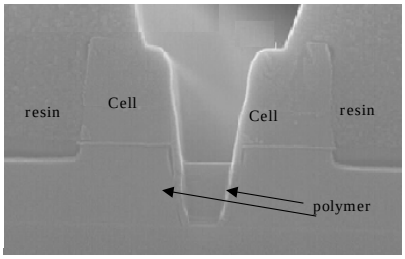

Figure 5: Flash cell after SAS etching, description of polymer

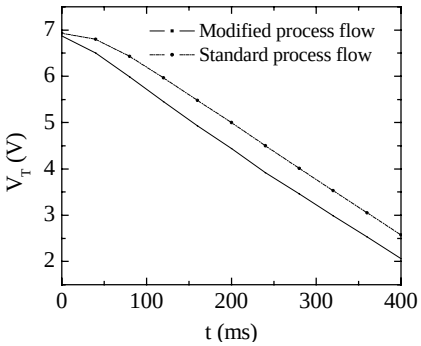

Figure 6: Measurments comparison of the threshold voltage between standard and modified process flow